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High-throughput manufacturing of epitaxial membranes from a single wafer by 2D materials-based layer transfer process

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Layer transfer techniques have been extensively explored for semiconductor device fabrication as a path to reduce costs and to form heterogeneously integrated devices. These techniques entail isolating epitaxial layers from an expensive donor wafer to form freestanding membranes. However, current layer transfer processes are still low-throughput and too expensive to be commercially suitable. Here we report a high-throughput layer transfer technique that can produce multiple compound semiconductor membranes from a single wafer. We directly grow two-dimensional (2D) materials on III–N and III–V substrates using epitaxy tools, which enables a scheme comprised of multiple alternating layers of 2D materials and epilayers that can be formed by a single growth run. Each epilayer in the multistack structure is then harvested by layer-by-layer mechanical exfoliation, producing multiple freestanding membranes from a single wafer without involving time-consuming processes such as sacrificial layer etching or wafer polishing. Moreover, atomic-precision exfoliation at the 2D interface allows for the recycling of the wafers for subsequent membrane production, with the potential for greatly reducing the manufacturing cost.

In recent years, the need for freestanding single-crystalline membranes of functional materials has been gaining much attention because implementations of these forms can provide extra degrees of freedom. For example, heterogeneous integration of dissimilar materials, which is not feasible by conventional heteroepitaxy, can be realized by stacking freestanding membranes[1]. By decoupling various types of epitaxial layers from donor wafers and integrating them together on a platform, the physical properties of dissimilar materials can be coupled resulting in membranes that, being unclamped from the substrate, are both flexible and lightweight[2]. More importantly, the adoption of freestanding membranes instead of bulky wafers provides significant cost savings for the production of devices, especially for non-silicon materials.

A variety of lift-off techniques, including chemical, optical and mechanical lift-off, have been developed for producing single-crystalline freestanding membranes and for reusing the costly wafer after the lift-off. However, each of these lift-off methods is applicable only to certain types of materials, and furthermore tend to damage or contaminate the substrate during the process, necessitating a thorough refurbishing step such as chemical-mechanical polishing (CMP). This not only adds substantially to the cost, but also limits the number of lift-off processes that can be conducted from a single wafer via recycling[3–7]. Thus, developing a process that can produce multiple single-crystalline membranes without the need for additional refurbishment is crucial to take full advantage of wafer recycling.

Recently, a two-dimensional (2D) materials-based layer transfer (2DLT) process, which employs 2D van der Waals (vdW) materials as an interfacial layer, has been proposed as an ultrafast mechanical lift-off technique, enabling precise exfoliation at the 2D interface due to the very weak adhesion between the vdW layer and the overlayer[8–10]. The overlayer can be epitaxially grown by remote epitaxy using graphene as a

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2D interlayer, which provides a path toward single-crystalline membrane production[9,11–14]. Although graphene should in principle be pristine for such atomically precise exfoliation, in many cases graphene is typically transferred from foreign templates onto the substrates of interest, inevitably generating defects in the graphene during the transfer process, such as tears, wrinkles and residues. This not only deteriorates the crystal quality of membranes grown by remote epitaxy but incurs local spalling from damaged areas of graphene during 2DLT[9]. Furthermore, because the host wafer does not remain atomically smooth after 2DLT due to such damage, refurbishing processes are still necessary to attain an epi-ready surface to reuse the wafer, like other lift-off techniques.

In this Article, we demonstrate a practical and universal method to grow and harvest epitaxial membranes with a high throughput at the wafer scale. We develop a technique to form multiple alternating layers of 2D materials and epitaxial films, where the epilayers are mechanically exfoliated by a layer-by-layer lift-off process with atomic precision, producing multiple freestanding membranes. After the epilayers are harvested by 2DLT, the wafer can be reused to repeat the process. Thus, we expect that this approach could substantially reduce the cost of non-silicon electronics by producing many copies of single-crystalline membranes from a single wafer.

Such a breakthrough is realized by the following key developments. First, we demonstrate a method to grow 2D materials directly on compound semiconductor wafers, such as III–N and III–V, in epitaxy tools at low temperatures so that surface dissociation can be avoided. As a result, III–N or III–V epilayers can be grown in the same epitaxy tool immediately after the formation of 2D materials. Second, wafer surfaces are undamaged during the peeling of epilayers, due to the damage-free 2D layers obtained by direct growth, which makes it possible to reuse the wafers without the need for CMP processes. Third, we expand the growth technique to form multiple stacks of epitaxial films with 2D interlayers by a single growth run. The III–V and III–N layers on wafers are then harvested by layer-by-layer peeling. With a nickel stressor deposited on top, the exfoliation occurs only from the topmost epilayer, realizing high-throughput and controllable lift-off of membranes with atomic-scale precision. Thus, the proposed membrane production process will open up opportunities to utilize materials solely based on their material properties without the burden of the wafer cost. Moreover, this technique will enable greater flexibility in designing heterostructures as well as in integrating inorganic semiconductor materials on non-flat surfaces for conformal electronics.

Direct growth of 2D materials

Figure 1a shows the process flow for harvesting multiple single-crystalline semiconductor membranes from a single wafer. One of the key developments to realize this high-throughput semiconductor membrane production is the transfer-free, direct formation of 2D materials on compound semiconductor wafers which can be conducted in situ with thin-film epitaxy. However, the high growth temperatures of 2D materials, such as graphene and hexagonal boron nitride (hBN), are one of the biggest challenges, since thermal desorption of III–V and III–N surfaces will occur during the growth of 2D layers[15,16]. To overcome this, we have developed a method to grow 2D materials on compound semiconductor wafers at a lower temperature that can minimize surface desorption. Low-temperature growth makes the crystal structure of 2D materials more defective but still with sp^2-dominant in-plane bonds, hereinafter named thin amorphous carbon (TAC) and boron nitride (BN) for simplicity.

We first show BN grown directly on GaN(0001) wafers by molecular beam epitaxy (MBE). Elemental boron and nitrogen plasma are used as sources for BN growth at 680 °C, which is a low enough temperature to prevent GaN surface desorption (see Methods for detailed growth conditions). As shown in the a1 copy (AFM) image (Fig. 1b), the GaN substrate coated with BN exhibits an average roughness (R_a) of 0.37 nm. X-ray photoelectron spectroscopy (XPS) measurements reveal the existence of boron and nitrogen peaks (Fig. 1c,d) although the nitrogen peak is from both the BN and GaN substrate. The shoulder peak at ~396 eV is attributed to the Auger peak of nitrogen from[17]. The absence of sideband peaks in Fig. 1c suggests that boron dominantly forms sp^2-bonds with nitrogen[18–20]. The plan-view high-resolution transmission electron microscopy (HRTEM) image of the BN layer in Fig. 1e shows that the BN layer is mostly in a nanocrystalline or amorphous phase due to the low growth temperature (see Methods for TEM specimen preparation process). We note that it is difficult to observe the exact crystallinity and thickness at the atomic scale because defective 2D materials are easily damaged or dissociated during TEM measurements.

We next show TAC growth directly on GaAs(001) wafers in a III–V metal–organic chemical vapour deposition (MOCVD) system at low temperature. Because GaAs is decomposed at an even lower temperature than GaN, a thin AlGaAs layer with a nominal aluminium composition of 50% ($Al_{0.5}Ga_{0.5}As$) is first grown on GaAs as a buffer that is thermally more robust and quasi-lattice-matched to GaAs. Next, using toluene as a carbon precursor with a low cracking temperature[21], TAC is formed on AlGaAs/GaAs substrates at 700 °C (see Methods for details). A similar set of characterization is conducted on TAC as BN, and the AFM measurements reveal a smooth TAC/AlGaAs/GaAs surface with an average roughness of 0.23 nm, as shown in Fig. 1f. The XPS spectra at the C 1*s* peak in Fig. 1g reveal a peak binding energy of ~285 eV without notable sideband peaks, indicating that carbon lattices are mostly sp^2-bonded. The Raman spectra of TAC (Fig. 1h), which are measured by transferring the TAC onto silicon substrates with a 300-nm-thick SiO_2 layer, show signature graphene peaks (G and 2D peaks) but with significant broadening. The broad 2D peak in Raman spectra and the slightly broad C 1*s* peak in XPS spectra agree perfectly with other reports on monolayer amorphous sp^2 carbon[22,23], which is also grown at a low temperature but not on III–V substrates. This suggests that the carbon layer formed on AlGaAs/GaAs is also in an amorphous sp^2 phase. The plan-view scanning TEM (STEM) image of freestanding TAC in Fig. 1i also confirms the defective/amorphous phase of the carbon layer.

Wafer-scale remote epitaxy and layer transfer

With the capability to form 2D layers on compound semiconductor wafers in epitaxy systems, a 'monolithic' remote epitaxy becomes possible, wherein 2D layers and epilayers are grown by a single growth run, without the need for 2DLT, sample loading/unloading or even a major change in temperature. The epitaxy of GaN can be conducted by first forming the BN layer on a GaN wafer at 680 °C and then directly ramping the temperature up to 700 °C for GaN growth. Similarly, AlGaAs buffer, TAC and remote epitaxial GaAs layer can all be grown by a single MOCVD run. Successful growths of GaN and GaAs thin films on these 2D layers are demonstrated in 2 inch GaN(0001) and 2 inch GaAs(001) wafer-scale. The cross-sectional STEM images in Fig. 2a,b clearly show epitaxially aligned GaN and GaAs epilayers with the substrate, with the presence of a dark gap due to BN and TAC interlayers, respectively. Because the growth of 2D materials on GaN and GaAs is not a self-limiting process, the thicknesses of BN and TAC are not completely monolayer. In addition, although the interfacial roughness of heterostructures and buckling of 2D materials make it difficult to estimate the thicknesses of 2D layers[22,24], the average thickness of BN shown in the STEM image is thicker than that of TAC. The impact of structural properties, such as thickness and crystallinity, of these 2D layers on the growth mode of GaN and GaAs are discussed further below and in Supplementary Note 1.

The plan-view scanning electron microscopy (SEM) images and electron backscatter diffraction (EBSD) maps of the top surfaces confirm that the epilayers are smooth and single-crystalline (Fig. 2c–f and Supplementary Fig. 1). However, the electron channelling contrast imaging (ECCI) results in the insets of Fig. 2c,d reveal that the GaN and GaAs surfaces exhibit dislocation densities of around 5×10^9 cm^{-2} and

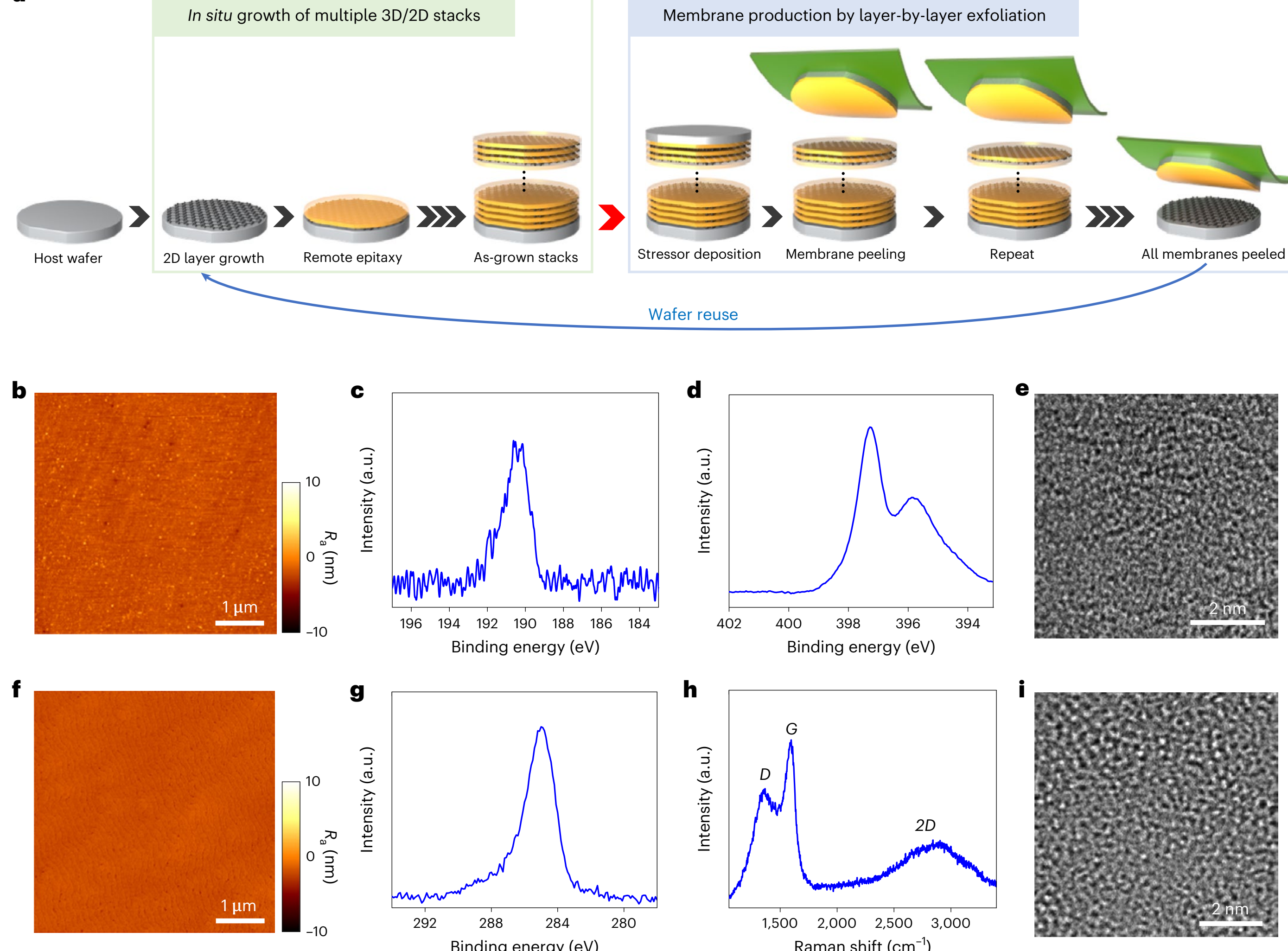

Fig. 1 | Direct growth of 2D materials for 2DLT. a, Schematic of the single-crystalline membrane production process by in situ growth of multiple stacks of epilayer/2D layer, layer-by-layer exfoliation with a stressor layer, and reuse of the substrate to repeat the process, maximizing the copies of membranes that can be produced from a single wafer. **b**–**d**, AFM image of BN formed on GaN substrate showing a smooth surface (**b**) and XPS measured around the B 1*s* peak (**c**) and the N 1*s* peak (**d**). **e**, Plan-view HRTEM image of a freestanding BN layer measured by transferring BN onto a TEM grid. **f**,**g**, AFM image of TAC formed on AlGaAs/GaAs substrate showing a smooth surface (**f**) and XPS spectra measured around the C 1*s* peak representing mostly sp^2-bonded characteristics (**g**). **h**, Raman spectra of TAC measured after transferring TAC onto SiO_2/Si substrate, which show three signature bands from graphene, namely, D, G, and 2D peaks. **i**, Plan-view STEM image of TAC measured by transferring TAC onto a TEM grid.

1×10^8 cm^{-2}, respectively. The relatively high dislocation density is attributed to the screening effect by 2D interlayers and the Volmer–Weber growth mode on 2D vdW surfaces. The quality of nucleation layers could be improved by optimizing the thickness and uniformity of the 2D materials and by optimizing the nucleation conditions of epilayers on 2D materials. Conventional dislocation reduction techniques, such as introducing thermal cycling annealing and strained buffer layers, could enhance the crystal quality of thin films further[25–27] (see Supplementary Note 2 for more discussion). Employing defect-tolerant device structures, such as quantum-dot-based active layers, will also make our approach more versatile[28,29].

Next, the grown films are exfoliated by 2DLT processes. A nickel stressor layer is deposited on the epilayer, followed by applying a thermal release tape (TRT) and then mechanically exfoliating the TRT/stressor/epilayer stack (see Methods for detailed 2DLT process). The photographs in Fig. 2g,h show exfoliated 2-inch-diameter GaN and GaAs membranes, confirming that directly grown 2D interlayers are indeed an effective platform for single-crystal membrane production.

One of the important questions is whether and how defective BN and carbon layers allow charge transfer to enable remote epitaxy, especially given that single-crystalline hBN allows only mixed-mode growth of quasi-vdW epitaxy and remote epitaxy[12]. Interestingly, our theoretical study by density functional theory (DFT) calculations reveals that charge transfer from GaN substrates to the surface of BN does not occur when BN is single-crystalline (that is, hBN), whereas partial transfer of charges is observed in the case of defective BN (Fig. 2i). In contrast, partial transfer of charges from GaAs substrates is observed from both graphene and TAC, as shown in Fig. 2j (see Methods, Supplementary Note 1 and Supplementary Figs. 2–5 for details). Defects in 2D materials can also promote quasi-vdW epitaxy modes[30], although our experimental results show no crystallographic relationship between epilayers and 2D materials (Supplementary Fig. 1), ruling out such a possibility. We note that other growth mechanisms or mixed growth modes may still play a role on defective BN, which is further discussed in Supplementary Note 1. Nevertheless, the experimental and theoretical studies substantiate that 2D materials directly grown

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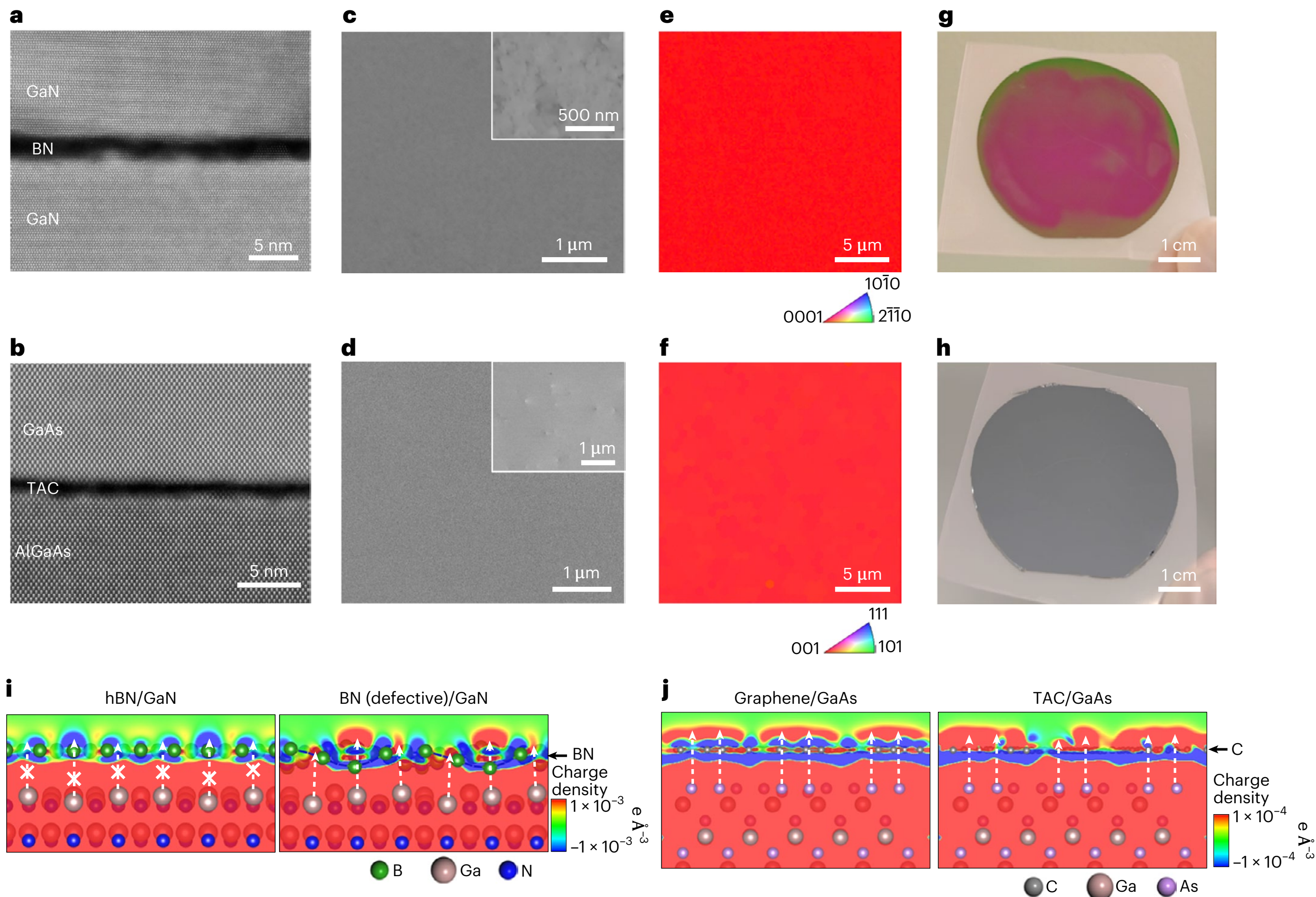

Fig. 2 | Remote epitaxy on directly grown 2D materials. a,**b**, Cross-sectional STEM images of 500-nm-thick GaN/BN (**a**) and 3-µm-thick GaAs/TAC/AlGaAs (**b**) grown on GaN(0001) and GaAs(001) substrates, respectively. **c**,**d**, Plan-view SEM images showing the surface morphology of GaN (**c**) and GaAs (**d**). Insets: ECCI images of surfaces, revealing a GaN dislocation density of around 5×10^9 cm^{-2} (**c**) and a GaAs dislocation density of around 1×10^8 cm^{-2} (**d**). **e**,**f**, EBSD maps of the top surfaces of GaN (**e**) and GaAs (**f**) membranes, confirming the single-crystallinity of the thin films. **g**,**h**, Photographs of exfoliated 2-inch-diameter single-crystal GaN membrane (**g**) and GaAs membrane (**h**). **i**,**j**, Cross-sectional images of charge density distribution induced by GaN substrates with BN (**i**) and GaAs substrates with graphene and TAC (**j**), which are calculated by subtracting the charge density induced by 2D materials from the total charge density. The arrows indicate charge transfer through the 2D layer. The arrows with crosses in hBN indicate that hBN completely screens the surface.

at low temperatures can be an effective platform for the growth of single-crystalline membranes that can be readily exfoliated.

Wafer recycling to produce multiple membranes

Such direct growth of 2D layers brings substantial advantages in that they form tear-free and residue-free layers on entire wafers. When 2D materials are transferred from foreign templates, on the other hand, (1) it is difficult to cover the entire area of wafers, (2) transfer-process-related residues and wrinkles deteriorate the quality of remote epitaxy[31,32], and (3) tearing of 2D materials inevitably occurs on the microscopic scales, from which direct epitaxy takes place, spalling the substrate during 2DLT[9]. All these challenges can be overcome by directly grown 2D layers, as evidenced by the successful release of full 2-inch-wafer-scale membranes as shown in Fig. 2g, h. Furthermore, as the wafers remain pristine without any damage, it is possible to reuse the wafer after peeling without the need for planarizing by CMP, which makes a clear contrast to conventional lift-off processes. In our approach, as schematically illustrated in Fig. 3a, wafer recycling is achieved simply by removing the remaining TAC or BN layer by O_2 plasma and then starting the process over.

As an example, we utilize the same GaAs wafer three times to produce three 2-inch-diameter GaAs membranes. The photographs in Fig. 3b show three GaAs membranes and the donor wafer after each peeling. The wafer surface characterized after each peeling shows virtually no degradation of substrates throughout the recycling process. Macroscopic spalling of the substrates is not observed in the SEM images (Fig. 3c), and the surface roughness measured by AFM is kept below 1 nm after undergoing the processes three times (Fig. 3d). The slight accumulation of nanoscopic damage in the AFM images is attributed to the unoptimized O_2 plasma treatment condition used for etching residual 2D layers. EBSD maps of exfoliated membranes in Fig. 3e show that the interface sides of the epilayers are single-crystalline, not just the top surfaces of the epilayer (Fig. 2e,f), corroborating the remote nucleation through TAC. The X-ray diffraction spectra of the 2θ–ω scan (2θ representing the angle between the incident X-ray beam and the detector, and ω representing the angle of incidence of the X-ray beam relative to the sample surface) for three exfoliated membranes (Fig. 3f) also confirm that the entire membranes are (001)-oriented.

The reusability of GaN wafers is also demonstrated by identical processes to GaAs wafer recycling, as shown in Supplementary Fig. 6. The slight damage near the edge of the GaAs wafer (Fig. 3b) is not an intrinsic issue of the process but due to the edge effect during the growth of TAC in our MOCVD reactor. We did not observe a difference in the quality of epilayers grown on recycled substrates versus fresh

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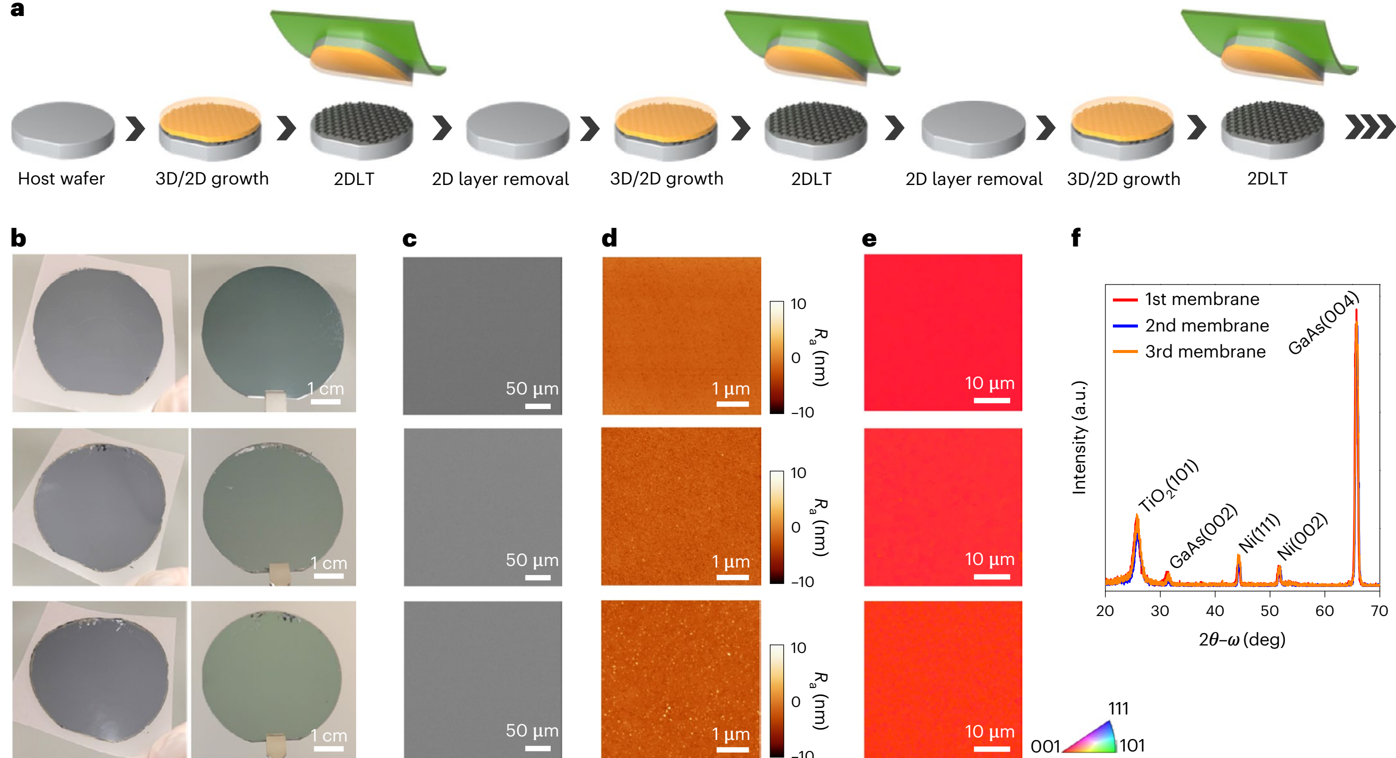

Fig. 3 | Multiple membrane production by reusing a wafer. a, Schematic of successive membrane production by remote epitaxy, 2DLT and wafer recycling. **b**–**e**, Characterization of exfoliated GaAs membranes and the substrate, conducted after each growth and 2DLT. Photographs of exfoliated membranes (**b**, left) and the remaining substrate (**b**, right), SEM images (**c**) and AFM images (**d**) of the substrate, and EBSD maps of the interface side of exfoliated GaAs membrane (**e**). The data in the upper, middle and lower rows correspond to the first, second and third growth and exfoliation from the same wafer, respectively. The roughness R_a in the AFM images is 0.42 nm (upper), 0.62 nm (middle) and 0.46 nm (lower). **f**, X-ray diffraction $2\theta-\omega$ scan of exfoliated membranes showing peaks from single-crystal GaAs(001) thin films and Ti/Ni stressors.

substrates (Supplementary Fig. 7). Therefore, directly grown 2D materials on compound semiconductor substrates can work as an effective template for wafer-scale remote epitaxy and wafer recycling.

Multistack growth and layer-by-layer exfoliation

The capability to directly form 2D materials on substrates of interest can uniquely enable the growth of multiple consecutive layers of 2D materials and 3D bulk layers by a single growth run, without the need for transferring 2D layers. The maximum number of such 3D/2D stacks that can be simultaneously grown is not limited in principle, and is only constrained by the epitaxial systems and practical growth durations. By growing multiple epilayers with 2D interlayers, it is possible to harvest many freestanding single-crystalline membranes by repeated mechanical exfoliation from the topmost layer (Fig. 1a), which is an extremely high-throughput process in terms of both the epitaxy and membrane harvest when compared with conventional layer lift-off techniques. Although an advanced epitaxial lift-off technique has been proposed by employing multiple sacrificial layers and transfer printing[33], isolation of each layer in these methods requires complex processes involving hole patterning/dry-etching, partial wet-etching, photoresist anchoring and final release, which are time-consuming and less practical. Furthermore, because the wafer can be reused in our approach without the need for CMP as demonstrated above, it has great potential for reducing manufacturing costs. Therefore, the proposed method represents a high-throughput and cost-effective approach for producing epitaxial membranes (see Supplementary Note 3 for more discussion).

As a proof-of-concept demonstration, we first perform the growth of three stacks of GaN/BN on GaN, by a single growth run in an MBE system. The SEM images in Fig. 4a,b confirm the successful growth of triple-stacked structures. The X-ray diffraction ϕ scan, wherein ϕ represents the rotation angle of the sample, of the as-grown structure in Fig. 4c shows sixfold symmetry, which confirms that all three GaN epilayers are crystallographically aligned with the GaN substrate. The single-crystallinity is also confirmed by the EBSD map in Fig. 4d measured at the interface side of the top layer. Similarly, three stacks of (Al)GaAs/TAC are grown on GaAs using an MOCVD system. In each stack, AlGaAs is grown below each TAC layer to prevent surface damage during the TAC growth. The same set of images in Fig. 4e–h confirms that crystallographically aligned single-crystalline GaAs layers are grown by a single growth run. It is also worth mentioning that we did not observe noticeable degradation of film quality by stacking up layers (Supplementary Figs. 8 and 9).

After the growth of multistacked epilayers, each layer can be exfoliated layer-by-layer using the same 2DLT process that is used for a single stack. Without additional efforts, the peeling occurs naturally at the topmost 2D interlayer, which can be intuitively understood considering that the bending stiffness, K, of thin films with the thickness, t, is proportional to $K \propto t^3$. In other words, if the interfacial toughness of all 2D interlayers is identical, it is energetically favourable for the topmost layer to be exfoliated under tensile strain, rather than more-than-one-layer being exfoliated simultaneously. Three-dimensional molecular dynamics (MD) simulations also confirm the case, in that only the topmost layer is exfoliated regardless of the total number of stacks (Fig. 4i) when tensile stress is applied by adding an additional stressor layer (see Methods, Supplementary Note 4, Supplementary Fig. 10 and Supplementary Video 1 for details). Experimentally, layer-by-layer peeling occurred by consecutive 2DLT processes for both GaN/BN stacks and GaAs/TAC stacks until the exposure of the substrate, as shown in Fig. 4i and Supplementary Fig. 11. Because GaN membranes are transparent, the non-uniform colour shown in the photographs of exfoliated membranes in Fig. 4i is a manifestation of Ti/Ni layers as viewed through

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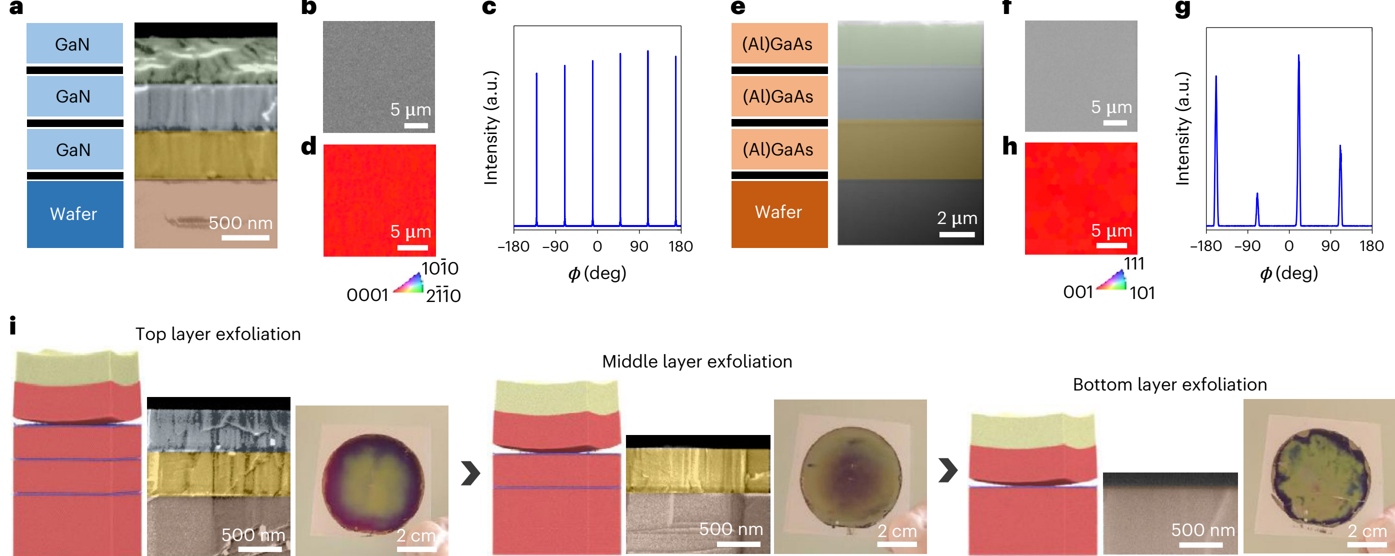

Fig. 4 | Multistack growth and layer-by-layer exfoliation. a, Schematic (left) and cross-sectional false-colour SEM image (right) of three stacks of GaN/BN grown on a GaN substrate. The rough sidewalls are formed because the sample is cleaved for imaging, which forms randomly fractured sidewalls near the surface. **b**, Plan-view SEM image of three stacks of GaN/BN grown on a GaN substrate. **c**,**d**, X-ray diffraction ϕ scan of the sample showing sixfold symmetry (**c**) and EBSD map measured at the interface side after exfoliation (**d**) confirming that all stacks are single-crystalline without in-plane rotation. **e**–**h**, The same set of data for GaAs/TAC. Thin AlGaAs layers are grown under each TAC layer. **i**, Layer-by-layer exfoliation of three stacks of GaN membranes: MD simulations (left), cross-sectional false-colour SEM images of the substrate after each exfoliation (centre) and photographs of exfoliated membranes (right) confirm the layer-by-layer exfoliation.

the GaN layers. After each peeling, exposed BN and TAC interlayers are removed by O_2 plasma before the next 2DLT process, so that the stressor layer is deposited on epilayers, not on 2D layers. After each exfoliation, surfaces of exposed epilayers and substrates remain pristine without mechanical damage (Supplementary Fig. 11). In addition, there was no degradation of epilayer material after transferring the exfoliated layer onto foreign substrates (Supplementary Fig. 9). These results exemplify the effectiveness of our approach in producing multiple freestanding membranes from multistacked epilayers.

Conclusion

We have demonstrated a method for producing single-crystalline semiconductor membranes with a high throughput potentially at a low cost. The key enabling technique is the formation of 2D materials directly on wafers by epitaxy tools, which allows for simultaneous growth of epilayers with 2D materials, and even multiple stacks of them. Using this technique, single or multiple stacks of 3D/2D layers are formed and then exfoliated by 2DLT processes, where the substrates can be reused for further production of membranes. We envision that this technique can be applied not only to III–V and III–N compound semiconductors, but also to many other materials by developing direct growth of 2D layers on various substrates. In particular, the available choice of materials can be further expanded if 2D layers can be grown at even lower temperatures than what we have shown here. Indeed, there are active studies on low-temperature growths of sp^2-bonded 2D layers, such as the growth of amorphous carbon and amorphous BN at temperatures as low as 200 °C[22] and 400 °C[34], respectively. Therefore, the proposed technique could become a universal method to produce single-crystalline membranes with great flexibility in the choice of materials for epilayers as well as substrates, benefiting diverse application fields of heterointegrated electronics and functional device platforms.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41565-023-01340-3.

References

1. Bae, S. H. et al. Integration of bulk materials with two-dimensional materials for physical coupling and applications. *Nat. Mater.* **18**, 550–560 (2019).
2. Kum, H. S. et al. Heterogeneous integration of single-crystalline complex-oxide membranes. *Nature* **578**, 75–81 (2020).
3. Cheng, C. W. et al. Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics. *Nat. Commun.* **4**, 1–7 (2013).
4. Wu, F. L., Ou, S. L., Horng, R. H. & Kao, Y. C. Improvement in separation rate of epitaxial lift-off by hydrophilic solvent for GaAs solar cell applications. *Sol. Energy Mater. Sol. Cells* **122**, 233–240 (2014).
5. Wong, W. S., Sands, T. & Cheung, N. W. Damage-free separation of GaN thin films from sapphire substrates. *Appl. Phys. Lett.* **72**, 599 (1998).
6. Raj, V. et al. Layer transfer by controlled spalling. *J. Phys. D* **46**, 152002 (2013).
7. Bedell, S. W., Lauro, P., Ott, J. A., Fogel, K. & Sadana, D. K. Layer transfer of bulk gallium nitride by controlled spalling. *J. Appl. Phys.* **122**, 025103 (2017).
8. Kobayashi, Y., Kumakura, K., Akasaka, T. & Makimoto, T. Layered boron nitride as a release layer for mechanical transfer of GaN-based devices. *Nature* **484**, 223–227 (2012).
9. Kim, Y. et al. Remote epitaxy through graphene enables two-dimensional material-based layer transfer. *Nature* **544**, 340–343 (2017).
10. Kim, H. et al. Graphene nanopattern as a universal epitaxy platform for single-crystal membrane production and defect reduction. *Nat. Nanotechnol.* **17**, 1054–1059 (2022).
11. Kum, H. et al. Epitaxial growth and layer-transfer techniques for heterogeneous integration of materials for electronic and photonic devices. *Nat. Electron.* **2**, 439–450 (2019).

12. Kong, W. et al. Polarity governs atomic interaction through two-dimensional materials. *Nat. Mater.* **17**, 999–1004 (2018).
13. Bae, S. H. et al. Graphene-assisted spontaneous relaxation towards dislocation-free heteroepitaxy. *Nat. Nanotechnol.* **15**, 272–276 (2020).
14. Kim, H. et al. Remote epitaxy. *Nat. Rev. Methods Prim.* **2:40**, 1–21 (2022).
15. Park, J.-H. et al. Influence of temperature-dependent substrate decomposition on graphene for separable GaN growth. *Adv. Mater. Interfaces* **6**, 1900821 (2019).
16. Koukitu, A., Mayumi, M. & Kumagai, Y. Surface polarity dependence of decomposition and growth of GaN studied using in situ gravimetric monitoring. *J. Cryst. Growth* **246**, 230–236 (2002).
17. Li, P., Xiong, T., Wang, L., Sun, S. & Chen, C. Facile Au-assisted epitaxy of nearly strain-free GaN films on sapphire substrates. *RSC Adv.* **10**, 2096–2103 (2020).
18. Kim, G. et al. Growth of high-crystalline, single-layer hexagonal boron nitride on recyclable platinum foil. *Nano Lett.* **13**, 1834–1839 (2013).
19. Jang, A. R. et al. Wafer-scale and wrinkle-free epitaxial growth of single-orientated multilayer hexagonal boron nitride on sapphire. *Nano Lett.* **16**, 3360–3366 (2016).
20. Bepete, G., Voiry, D., Chhowalla, M., Chiguvare, Z. & Coville, N. J. Incorporation of small BN domains in graphene during CVD using methane, boric acid and nitrogen gas. *Nanoscale* **5**, 6552–6557 (2013).
21. Zhang, B. et al. Low-temperature chemical vapor deposition growth of graphene from toluene on electropolished copper foils. *ACS Nano* **6**, 2471–2476 (2012).
22. Toh, C. T. et al. Synthesis and properties of free-standing monolayer amorphous carbon. *Nature* **577**, 199–203 (2020).
23. Joo, W. J. et al. Realization of continuous Zachariasen carbon monolayer. *Sci. Adv.* **3**, e1601821 (2017).
24. Zhang, Y. T. et al. Structure of amorphous two-dimensional materials: elemental monolayer amorphous carbon versus binary monolayer amorphous boron nitride. *Nano Lett.* **22**, 8018–8024 (2022).
25. Jung, D. et al. Low threading dislocation density GaAs growth on on-axis GaP/Si (001). *J. Appl. Phys.* **122**, 225703 (2017).
26. Shang, C. et al. A pathway to thin GaAs virtual substrate on on-axis Si (001) with ultralow threading dislocation density. *Physica Status Solidi A* **218**, 2000402 (2021).
27. Hool, R. D. et al. Challenges of relaxed n-type GaP on Si and strategies to enable low threading dislocation density. *J. Appl. Phys.* **130**, 243104 (2021).
28. Liu, A. Y. et al. High performance continuous wave 1.3 μm quantum dot lasers on silicon. *Appl. Phys. Lett.* **104**, 041104 (2014).
29. Chen, S. et al. Electrically pumped continuous-wave III–V quantum dot lasers on silicon. *Nat. Photonics* **10**, 307–311 (2016).
30. Liang, D., Wei, T., Wang, J. & Li, J. Quasi van der Waals epitaxy nitride materials and devices on two dimension materials. *Nano Energy* **69**, 104463 (2020).
31. Kim, H. et al. Role of transferred graphene on atomic interaction of GaAs for remote epitaxy. *J. Appl. Phys.* **130**, 174901 (2021).
32. Kim, H. et al. Impact of 2D–3D heterointerface on remote epitaxial interaction through graphene. *ACS Nano* **15**, 10587–10596 (2021).
33. Yoon, J. et al. GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies. *Nature* **465**, 329–333 (2010).
34. Hong, S. et al. Ultralow-dielectric-constant amorphous boron nitride. *Nature* **582**, 511–514 (2020).

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Methods

MBE growth of BN and III–N

BN and GaN are grown in a Veeco Gen200 plasma-assisted MBE system. GaN-on-sapphire (0001) wafers (2 inch, 4 μm; MSE Supplies) are used. Prior to growth, wafers are cleaned by first immersing in acetone at 75 °C for 15 min, followed by isopropanol at 75 °C for 15 min and blow-drying. Next, the wafers are immersed in dilute HCl (33 vol% in deionized water) for 15 min and blow-dried with nitrogen immediately before loading into the MBE chamber. BN is grown by a high-temperature boron effusion source and plasma-assisted nitrogen source at 680 °C substrate temperature and under a nitrogen-rich condition for around 1 h. After the growth of BN, the substrate temperature is ramped up to 700 °C for GaN growth. GaN is grown by a high-temperature gallium effusion source and plasma-assisted nitrogen source under a gallium-rich condition. A nominally 40-nm-thick GaN nucleation layer is first grown under a nitrogen-rich condition for around 10 min, to prevent the formation of Ga droplets which could damage the BN layer. Then, the gallium flux is ramped up for full growth under a typical gallium-rich condition with a growth rate of ~5 nm min^{-1}. For multistack growth runs, the substrate is kept at 700 °C with only a nitrogen source for 2 min after the GaN growth to evaporate gallium droplets on the surface for the next BN layer growth.

MOCVD growth of TAC and III–V

TAC, AlGaAs and GaAs are grown in a Thomas Swan close-coupled showerhead MOCVD reactor using toluene, arsine, trimethylgallium and trimethylaluminium as sources of carbon, arsenic, gallium and aluminium, respectively. Epi-ready 2 inch GaAs (001) wafers (AXT) are kept in an MOCVD glovebox and loaded directly to the MOCVD reactor without a cleaning process. In all growths, double-purified nitrogen is used as a carrier gas and the reactor pressure was kept at 100 torr. First, 100-nm-thick GaAs buffer for nucleation and 200- to 300-nm-thick AlGaAs for a thermal buffer are grown at 700 °C. The composition of AlGaAs is nominally $Al_{0.5}Ga_{0.5}As$. TAC is then grown at around 700 °C by flowing toluene into the reactor and shutting off both group III and group V precursors for around 10–15 min. Next, GaAs is grown by two-step growth, with low-temperature nucleation at around 500 °C followed by full growth at 650 °C with a V/III flow rate ratio of ~45 and a growth rate of ~33 nm min^{-1}. The growth of TAC and GaAs can be conducted either in a single growth run or by two separate runs, without notable difference in the results. After the growth, the reactor is cooled down with arsine flow to prevent surface desorption.

Exfoliation of epilayers

The 2DLT process of GaN and GaAs epilayers is conducted by first depositing a metal stressor layer. A 30-nm-thick titanium adhesion layer is deposited on as-grown samples by e-beam evaporation, followed by 2- to 5-μm-thick nickel deposition using d.c. sputtering under argon ambient. After the deposition of titanium/nickel, a TRT (semiconductor equipment) is attached to the nickel. Finally, the TRT/Ni/Ti/epilayer stack is released by lifting up the tape from the edge of the stack. For wafer recycling or layer-by-layer exfoliation of multistacked structures, exposed 2D interlayer (BN or TAC) is removed by O_2 plasma after exfoliation for subsequent processes.

Characterizations

XPS spectra of BN and TAC are measured with a magnesium Kα source (MultiLab 2000, Thermo VG) at room temperature. SEM and EBSD images are measured using a Zeiss Merlin high-resolution SEM system. SEM images are acquired at an acceleration voltage of 3 kV and a current of 100 pA. EBSD images are obtained at 15 kV and 3 nA using an EBSD detector in the microscopy system. AFM images are obtained using a Park NX10 system (Park Systems) with a non-contact probe (PPP-NCHR, Nanosensors). For Raman spectroscopy of TAC, the TAC layer is first transferred onto 300-nm-thick SiO_2/Si substrates by a dry-transfer process, the detailed procedure for which is reported elsewhere[32]. Raman spectra are measured using a Renishaw Invia Reflex Micro Raman system (α 300M+, 520 WITec) with a pump laser wavelength of 532 nm. X-ray diffration characterization is performed with a Bruker D8 high-resolution diffractometer with a Cu Kα1 source and a Ge (022) incident beam monochromator. We note that measuring spectral linewidths of exfoliated membranes is prone to peak broadening due to the bowing of membranes by stressor layers.

HRTEM and STEM measurements

For plan-view imaging of BN and TAC, (S)TEM specimens are prepared by the following processes. First, as-grown 2D layers are transferred onto silicon substrates with 300-nm-thick thermal SiO_2, by 2D materials dry transfer processes that are described elsewhere[14]. The BN and TAC layers on SiO_2/Si substrates are then transferred onto TEM grids by a standard wet transfer process[14] that involves spin-coating the substrate with polymethyl methacrylate (PMMA), immersing the PMMA-coated sample in dilute hydrofluoric acid to etch SiO_2 and cause a PMMA/2D stack float up, transferring the PMMA/2D stack to deionized water, and then scooping the stack with a TEM grid in deionized water. Finally, PMMA is removed with acetone vapour and the TEM grid with 2D materials is ready for imaging. Plan-view images are collected using a JEOL JEM-ARM200F TEM equipped with an image corrector, a cold field emission gun and a Gatan OneView camera, operated at 80 kV for HRTEM and 220 kV/86 pA for high-angle annular dark-field STEM. Cross-sectional STEM specimens are prepared by a conventional focused ion beam lift-out technique using a Helios NanoLab 600 and an FEI Helios 660. Cross-sectional STEM images are acquired using Thermo Fisher Scientific Themis Z S/TEM operated at 200–300 kV.

MD simulations

Molecular dynamics simulations are carried out with the LAMMPs[35,36] package where the equations of motion are integrated using the velocity-Verlet algorithm under a time step of 1 fs. To mimic the behaviour of Ge–Si–C systems, the Stillinger–Weber potential parameterized by Ethier and Lewis[37] was used here. The interaction of carbon atoms within the graphene layer is also described by the Stillinger–Weber potential, parameterized by Bourque and Rutledge[38]. Further details of the simulation set-up and discussion are given in Supplementary Note 4.

DFT calculations

DFT calculations are conducted with the generalized gradient approximation using the Vienna Ab initio Simulation Package[39–41]. The projector augmented wave potentials are employed to describe the potentials from the atom centres as implemented in the Vienna Ab initio Simulation Package. The energy cutoff for the plane-wave basis is set to 400 eV. All geometries are optimized until the Hellman–Feynman forces acting on the atoms become smaller than 0.03 eV $Å^{-1}$. To include weak vdW interactions between graphene (or TAC)/GaAs(001) and between BN/GaN interfaces, we adopt Grimme's DFT-D3 vdW corrections based on a semiempirical generalized gradient approximation-type theory[42]. For the Brillouin-zone interaction, we use a 3 × 3 × 1 grid in a Monkhorst–Pack special *k*-point scheme. Further details of the set-up and discussion are given in Supplementary Note 1.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

35. Plimpton, S. Fast parallel algorithms for short-range molecular dynamics. *J. Comput. Phys.* **117**, 1–19 (1995).
36. Zhang, Y., Huang, L. & Shi, Y. Silica glass toughened by consolidation of glassy nanoparticles. *Nano Lett.* **19**, 5222–5228 (2019).

37. Ethier, S. & Lewis, L. J. Epitaxial growth of $Si_{1-x}Ge_x$ on Si(100)2×1: a molecular-dynamics study. *J. Mater. Res.* **7**, 2817–2827 (1992).
38. Bourque, A. J. & Rutledge, G. C. Empirical potential for molecular simulation of graphene nanoplatelets. *J. Chem. Phys.* **148**, 144709 (2018).
39. Kresse, G. & Furthmüller, J. Efficient iterative schemes for ab initio total-energy calculations using a plane-wave basis set. *Phys. Rev. B* **54**, 11169 (1996).
40. Kresse, G. & Furthmüller, J. Efficiency of ab-initio total energy calculations for metals and semiconductors using a plane-wave basis set. *Comput. Mater. Sci.* **6**, 15–50 (1996).
41. Perdew, J. P., Burke, K. & Ernzerhof, M. Generalized gradient approximation made simple. *Phys. Rev. Lett.* **77**, 3865 (1996).
42. Grimme, S., Antony, J., Ehrlich, S. & Krieg, H. A consistent and accurate ab initio parametrization of density functional dispersion correction (DFT-D) for the 94 elements H–Pu. *J. Chem. Phys.* **132**, 154104 (2010).

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Author contributions

Jeehwan Kim conceived the idea and led the research. H.K., Y.L., K. Lu, C.S.C., K.Q. and W.K. designed the experiments. Y.L., K.Q., B.-I.P., Jekyung Kim and J.J. conducted III–N and BN growth. H.K., K. Lu and N.M.H. conducted III–V growth. H.K., K. Lu., N.M.H., K.S.K., S.L., C.K., H.W., L.K. and J. Kong developed TAC growth. D.S., H.-K.C. and S.H. conducted DFT calculations. M.A., Y.Z. and Y.S. conducted MD simulations. C.S.C., M.Z., K.S.K., S. Kang, J.P., S. Kim and J.H. conducted (S)TEM measurements. H.K., Y.L., K. Lu, C.S.C., C.C., X.Z. and S.-H.B. conducted 2DLT and 2D materials transfer. H.K., Y.L., K. Lu, K.Q., K.S.K., J.M.S., Y.B., Y.J.J., N.N.A., M.N.M.A., K. Lee and G.Y.Y. conducted characterization of thin films, BN and TAC. The manuscript was written by H.K. and Jeehwan Kim with input from all authors. All authors contributed to the analysis and discussion of the results leading to the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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